Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:
forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;
patterning said laminated structure into at least one gate stack extending from said substrate;
forming spacers adjacent said gate stack;
doping regions of said substrate not protected by said spacers to form source and drain regions adjacent said gate stack; and
removing said spacers and said sacrificial layer.

[c2] The method in claim 1, wherein the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers.

[c3] The method in claim 1, wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone.

[c4] The method in claim 3, wherein said larger spacing positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

[c5] The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising:
forming a sacrificial oxide layer above said gate conductor, and
forming additional sacrificial layers above said oxide layer

[c6] The method in claim 5, wherein said sacrificial oxide layer protects said gate conductor.

[c7] The method in claim 1, wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and
whereas, without said sacrificial layer, said doping pro-

cess would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer.

[c8] The method in claim 1, wherein said laminated structure includes a silicon layer below said gate conductor,
wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process,
wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,
wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and
whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer.

[c9] A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:
forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;
patterning said laminated structure into at least one gate

stack extending from said substrate;
forming spacers adjacent said gate stack;
epitaxially growing raised source and drain regions on said substrate adjacent said gate stack;
implanting impurities into said raised source and drain regions and into said substrate; and
removing said spacers and said sacrificial layer.

[c10] The method in claim 9, wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone.

[c11] The method in claim 10, wherein said larger spacing positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor.

[c12] The method in claim 9, wherein said sacrificial layer above said gate conductor is formed in a process comprising:
forming a sacrificial oxide layer above said gate conductor, and
forming additional sacrificial layers above said oxide layer,

wherein said sacrificial oxide layer protects said gate conductor.

[c13] The method in claim 9, wherein said laminated structure includes a silicon layer below said gate conductor,
wherein said method further comprises doping said source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process,
wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and
whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer.

[c14] The method in claim 9, wherein said laminated structure includes a silicon layer below said gate conductor,
wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process,
wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and
whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer.

[c15] The method in claim 9, wherein by implanting said impurities after said epitaxially growing process, said impurities avoid being subjected to the thermal budget of said epitaxially growing process.

[c16] A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:
forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;
patterning said laminated structure into at least one gate stack extending from said substrate;
epitaxially growing raised source and drain regions on said substrate adjacent said gate stack, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;
implanting impurities into said raised source and drain regions and into said substrate,
removing said spacers and said sacrificial layer.

[c17] The method in claim 16, wherein the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers.

[c18] The method in claim 16, wherein the size of said spacers is controlled by the combined height of said gate conductor and said sacrificial layer, such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone.

[c19] The method in claim 18, wherein said larger spacing positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

[c20] The method in claim 16, wherein said sacrificial layer above said gate conductor is formed in a process comprising:
forming a sacrificial oxide layer above said gate conductor, and
forming additional sacrificial layers above said oxide layer.

[c21] The method in claim 20, wherein said sacrificial oxide layer protects said gate conductor.

[c22] The method in claim 16, wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises doping said source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process,
wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and
whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and gate dielectric layer to said silicon layer.

[c23] The method in claim 16, wherein said laminated structure includes a silicon layer below said gate conductor, wherein said method further comprises a first doping process of doping source/drain electrodes and said gate conductor together in a self-aligned implantation after said patterning process,
wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity that used in said first doping process after said first doping process,
wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching

said silicon layer, and
whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer.

[c24] A method of producing an integrated circuit transistor comprising:
forming a laminated stack deposition, wherein said laminated stack deposition is formed in a process comprising:
forming a silicon layer over a substrate layer;
forming a gate oxide on said silicon layer;
forming a gate conductor on said gate oxide; and
forming of least one sacrificial material above said gate conductor,
patterning said gate oxide, gate conductor, and said sacrificial material into at least one gate stack;
forming temporary spacers adjacent said gate stack;
epitaxially growing raised source and drain regions above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack;
growing an additional dielectric layer on said raised source and drain regions;
removing said temporary spacers without removing said sacrificial material;

performing a halo implant in said raised source and drain regions and in exposed regions of said silicon layer;
forming a permanent spacer adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer;
implanting impurities into said raised source and drain regions and exposed regions of said silicon;
forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions;
implanting additional impurities into said raised source and drain regions and exposed regions of said silicon;
annealing to activate all impurities;
etching back said additional dielectric layer on said raised source and drain regions; and
saliciding both said gate conductor and said raised source and drain regions.

[c25] The method in claim 24, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities.

[c26] The method in claim 24, wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers.

[c27] The method in claim 24, wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer.

[c28] The method in claim 31, wherein said sacrificial oxide layer protects said gate conductor.